FIG. 1

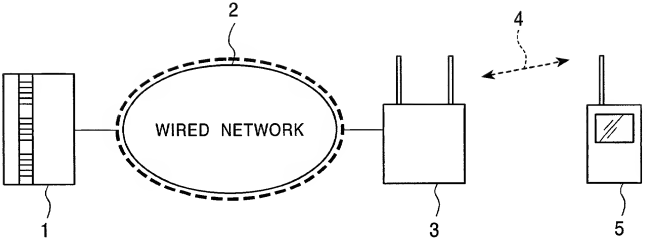

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FIG. 2

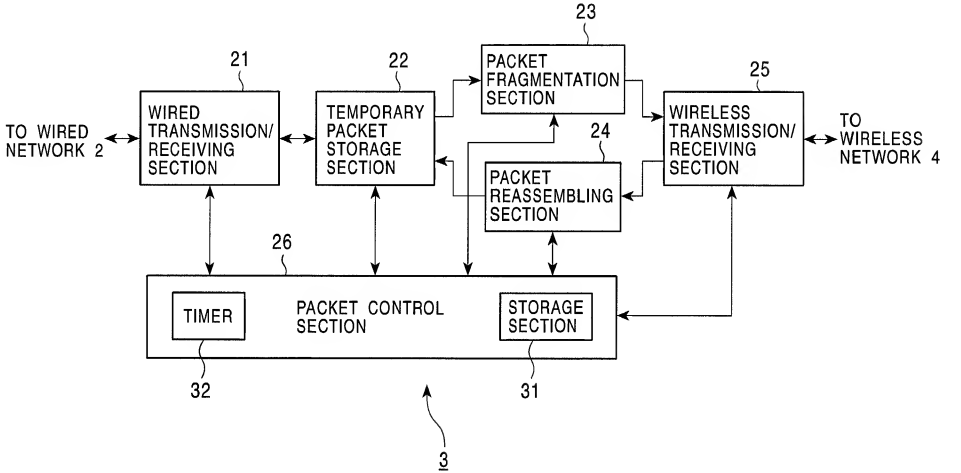
23
21
22
PACKET FRAGMENTATION SECTION
25
TO WIRED NETWORK 2
WIRED TRANSMISSION/ RECEIVING SECTION
TEMPORARY PACKET STORAGE SECTION
24
WIRELESS TRANSMISSION/ RECEIVING SECTION
TO WIRELESS NETWORK 4
PACKET REASSEMBLING SECTION
26
TIMER
PACKET CONTROL SECTION
STORAGE SECTION
32
31
3

FIG. 3

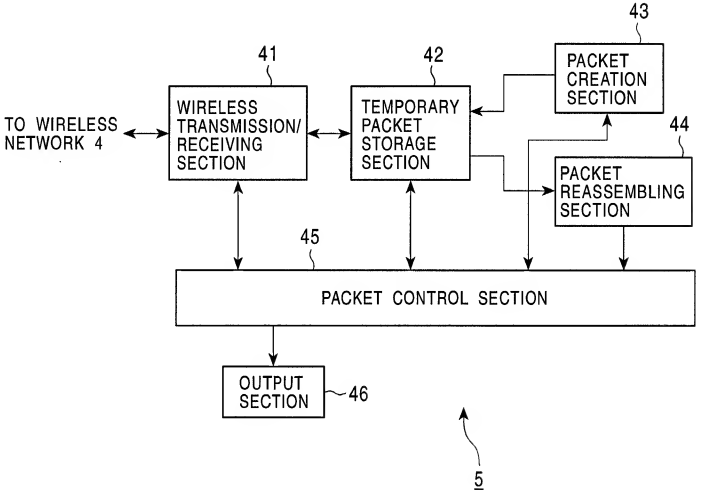
43
41
42
PACKET CREATION SECTION
TO WIRELESS NETWORK 4
WIRELESS TRANSMISSION/ RECEIVING SECTION
TEMPORARY PACKET STORAGE SECTION
44
PACKET REASSEMBLING SECTION
45
PACKET CONTROL SECTION
OUTPUT SECTION
46
5

FIG. 4

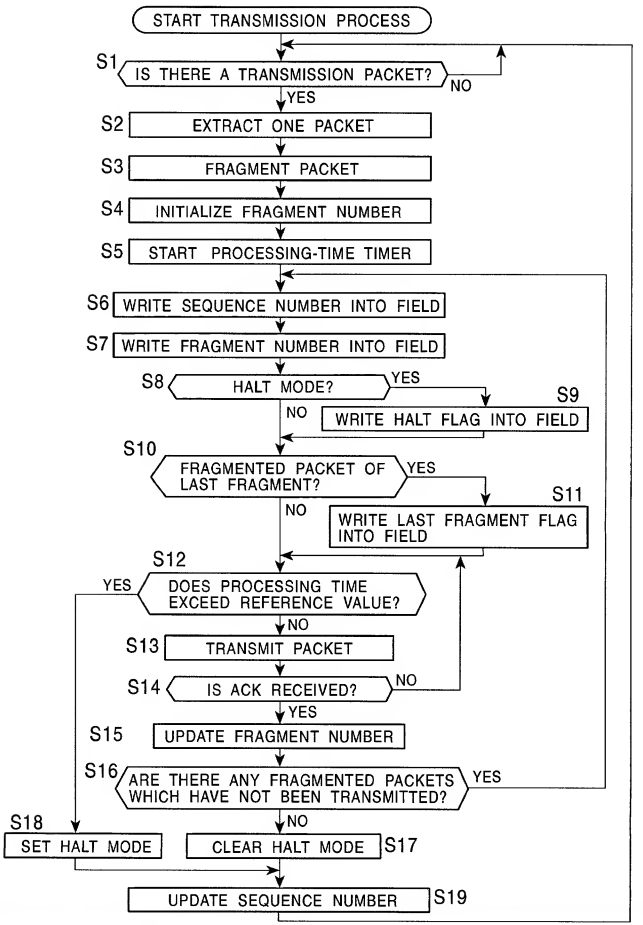

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FIG. 5

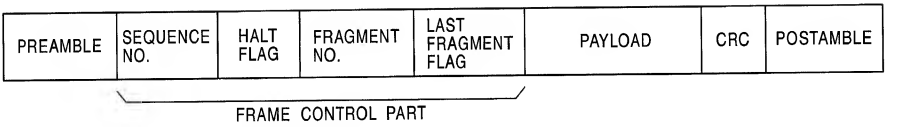


FIG. 6

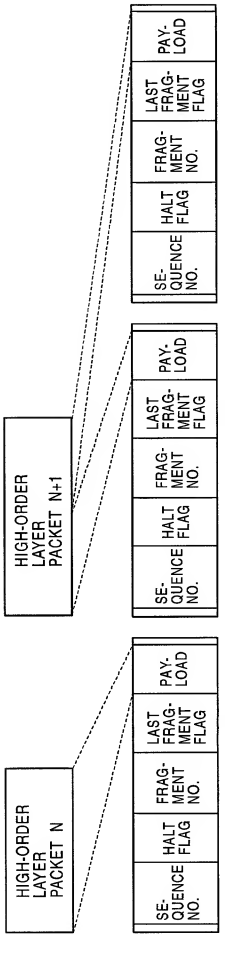

HIGH-ORDER LAYER PACKET N
HIGH-ORDER LAYER PACKET N+1
SE-QUENCE NO.
HALT FLAG
FRAG-MENT NO.
LAST FRAG-MENT FLAG
PAY-LOAD
[1]
[N]
[1]
[Y]
[2]
[N]
[1]
[N]
[2]
[N]
[2]
[Y]

FIG. 7

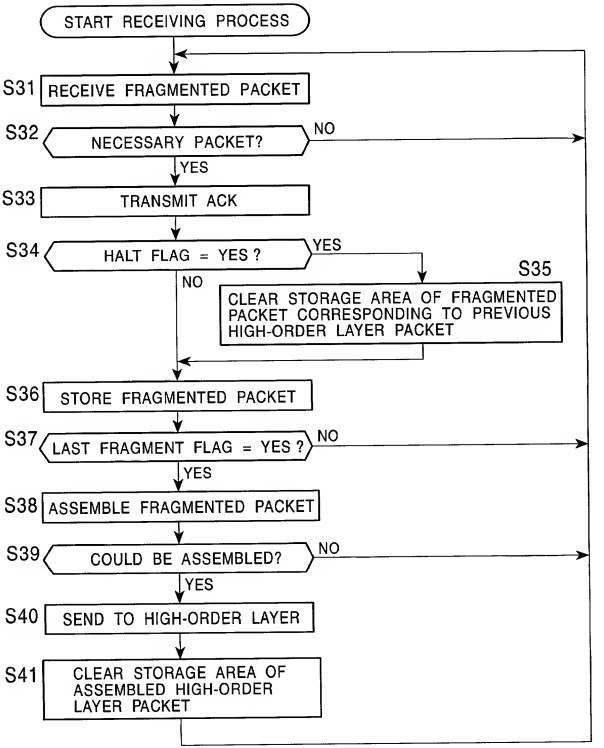

START RECEIVING PROCESS
S31
RECEIVE FRAGMENTED PACKET
S32
NECESSARY PACKET?
NO
YES
S33
TRANSMIT ACK
S34
HALT FLAG = YES ?
YES
NO
S35
CLEAR STORAGE AREA OF FRAGMENTED PACKET CORRESPONDING TO PREVIOUS HIGH-ORDER LAYER PACKET
S36
STORE FRAGMENTED PACKET
S37
LAST FRAGMENT FLAG = YES ?
NO
YES
S38
ASSEMBLE FRAGMENTED PACKET
S39
COULD BE ASSEMBLED?
NO
YES
S40
SEND TO HIGH-ORDER LAYER
S41
CLEAR STORAGE AREA OF ASSEMBLED HIGH-ORDER LAYER PACKET

FIG. 8

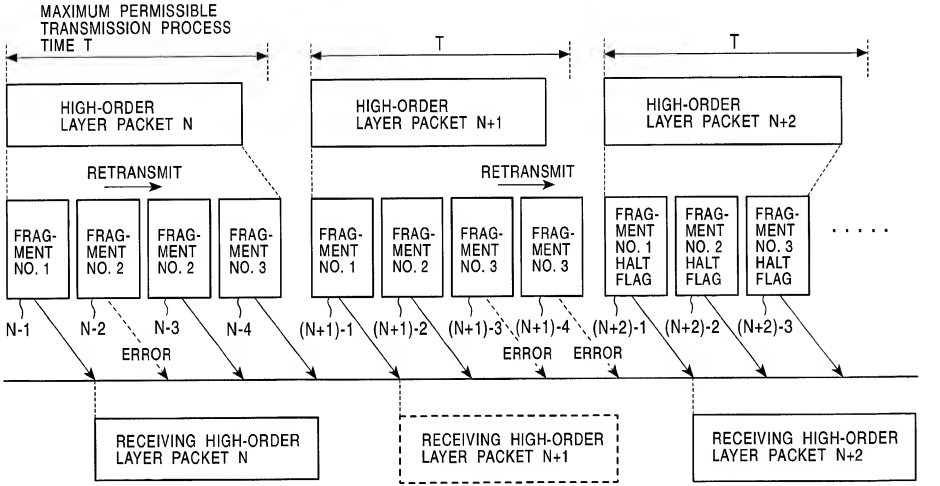
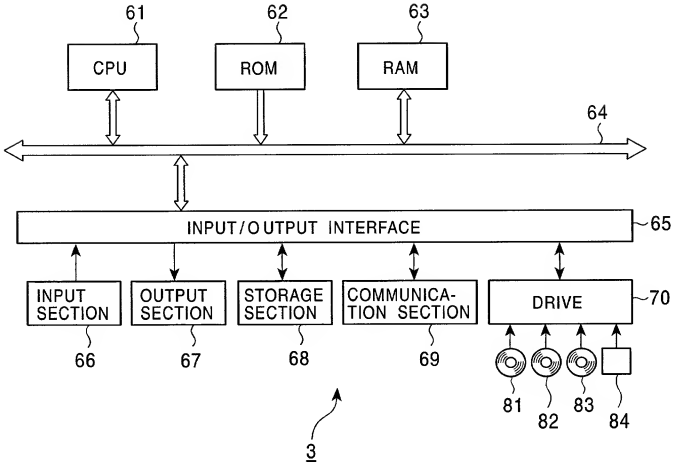

MAXIMUM PERMISSIBLE TRANSMISSION PROCESS TIME T
T
T
HIGH-ORDER LAYER PACKET N
HIGH-ORDER LAYER PACKET N+1
HIGH-ORDER LAYER PACKET N+2
RETRANSMIT
RETRANSMIT
FRAG-MENT NO. 1
FRAG-MENT NO. 2
FRAG-MENT NO. 2
FRAG-MENT NO. 3
FRAG-MENT NO. 1
FRAG-MENT NO. 2
FRAG-MENT NO. 3
FRAG-MENT NO. 3
FRAG-MENT NO. 1 HALT FLAG
FRAG-MENT NO. 2 HALT FLAG
FRAG-MENT NO. 3 HALT FLAG
N-1
N-2
N-3
N-4
(N+1)-1
(N+1)-2
(N+1)-3
(N+1)-4
(N+2)-1
(N+2)-2
(N+2)-3
ERROR
ERROR
ERROR
RECEIVING HIGH-ORDER LAYER PACKET N
RECEIVING HIGH-ORDER LAYER PACKET N+1
RECEIVING HIGH-ORDER LAYER PACKET N+2

FIG. 9


61
62
63
CPU
ROM
RAM
64
INPUT/OUTPUT INTERFACE
65
INPUT SECTION
OUTPUT SECTION
STORAGE SECTION
COMMUNICATION SECTION
DRIVE
70
66
67
68
69
81
82
83
84
3